IN THE CLAIMS

1. (Currently amended) A universal interface device, comprising:

a controller;

a configuration database coupled to the controller, said configuration database having stored therein a plurality of different configuration protocols for supporting a plurality of different peripheral devices;

a plurality of interconnection pads;

a memory coupled to the interconnection pads and controller, the memory is programmable by the controller in order to support any of the different peripheral devices; and

a multiplexer coupled between the memory and the plurality of interconnection pads wherein the universal interface device concurrently interfaces with the plurality of different peripheral devices using time division multiplexing of the plurality of interconnection pads.

2. (Original) A universal interface device as defined in claim 1, wherein the controller comprises a state machine.

R1.126 ~~4.~~ 3. (Original) A universal interface device as defined in claim 1, further comprising a programmable clock coupled to the memory or the configuration database.

R.1.26 ~~5.~~ 4. (Original) A universal interface device as defined in claim 1, wherein the controller selects a configuration protocol from amongst the plurality of configuration protocols in the configuration database, and uses the selected configuration protocol to configure the memory in order to support the peripheral

device from amongst the plurality that is coupled to the plurality of interconnection pads.

RI.126 5. ~~6.~~ (Original) A universal interface device as defined in claim 2, wherein the state machine includes a programmable routing and mapping scheme that allows the state machine to communicate with more than one peripheral device that is coupled to the plurality of interconnection pads.

RI.126 6. ~~8.~~ (Original) A universal interface as defined in claim 2, wherein the memory can be divided up by the state machine into two or more parts in order to support a peripheral device coupled to the interconnection pads that requires continuous transfer of data, the state machine switching between the two or more parts of the memory during data transfer to the peripheral device.

RI.126 7. ~~9.~~ (Original) A universal interface as defined in claim 2, wherein the state machine sets a portion of the memory to provide a tri-state control if one or more of the plurality of interconnection pads have to function as both an input and an output.